



# 1011LD110A

110 Watts, 32 Volts

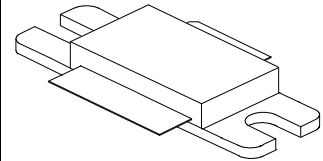
Pulsed Avionics 1030 to 1090 MHz

LDMOS FET

## GENERAL DESCRIPTION

The 1011LD110A is a COMMON SOURCE N-Channel enhancement mode lateral MOSFET capable of providing 110W<sub>pk</sub> of RF power from 1030MHz to 1090 MHz. The device is nitride passivated and utilizes gold metallization to ensure highest MTTF. The transistor includes input and output prematch for broadband capability. Low thermal resistance package reduces junction temperature, extends life. Integrated ESD protection makes the device robust.

**CASE OUTLINE**  
**55QZ**  
**(Common Source)**



## ABSOLUTE MAXIMUM RATINGS

### Voltage and Current

Drain-Source ( $V_{DS}$ ) +65V  
 Gate-Source ( $V_{GS}$ ,  $V_{DS}=0$ ) +20V

### Temperatures

Storage Temperature -65 to +150°C  
 Operating Case Temperature<sup>1</sup> +100°C

## ELECTRICAL CHARACTERISTICS @ 25°C

| SYMBOL          | CHARACTERISTICS              | TEST CONDITIONS                | MIN | TYP | MAX  | UNITS   |
|-----------------|------------------------------|--------------------------------|-----|-----|------|---------|
| $BV_{DSS}$      | Drain-Source Breakdown       | $V_{GS} = 0V$ , $I_D = 2mA$    | 65  |     |      | V       |
| $I_{DSSF}$      | Drain-Source Leakage Current | $V_{DS} = 32V$ , $V_{GS} = 0V$ |     |     | 5    | $\mu A$ |
| $I_{GSSF}$      | Gate-Source Leakage Current  | $V_{GS} = 10V$ , $V_{DS} = 0V$ |     |     | 2    | $\mu A$ |
| $V_{GS(TH)}$    | Gate Threshold Voltage       | $V_{DS} = 10V$ , $I_D = 3mA$   | 2   |     | 4    | V       |
| $V_{DS(ON)}$    | Drain-Source On Voltage      | $V_{GS} = 10V$ , $I_D = 1A$    |     |     | 0.25 | V       |
| $g_{FS}$        | Forward Transconductance     | $V_{DS} = 10V$ , $I_D = 1A$    |     | 2.2 |      | S       |
| $\theta_{JC}^1$ | Thermal Resistance           |                                |     |     | 0.1  | °C/W    |

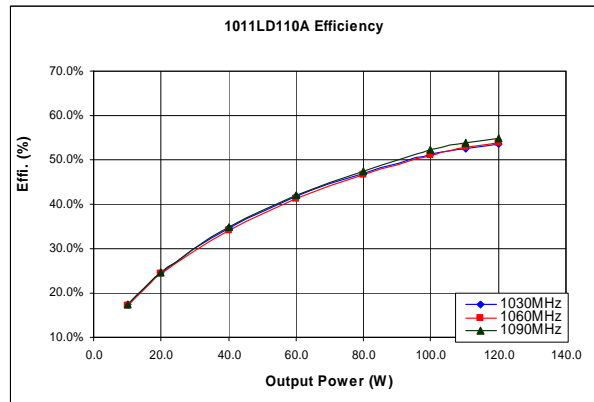
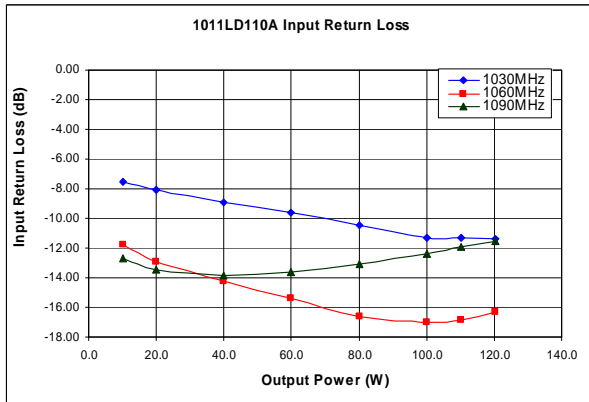
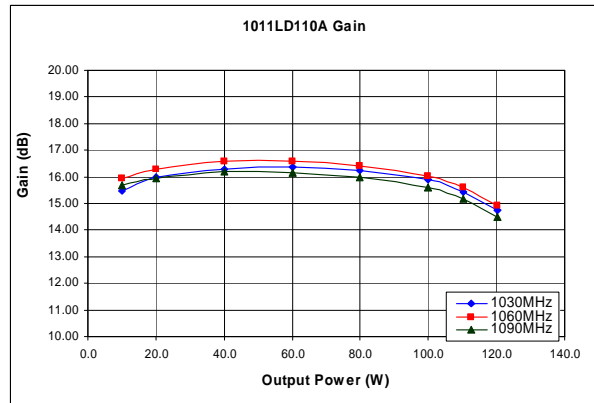
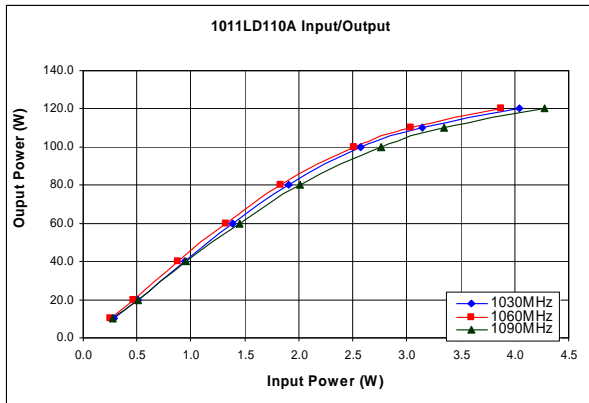
## FUNCTIONAL CHARACTERISTICS @ 25°C, $V_{ds} = 32V$ , $I_{DQ} = 250mA$

|           |                                      |   |    |     |     |    |
|-----------|--------------------------------------|---|----|-----|-----|----|
| $G_{PS}$  | Common Source Power Gain             | Pulse width = 32 $\mu s$ , LTDC=2%                  | 14 | 15  |     | dB |
| $P_d$     | Pulse Droop                          | F=1030/1090 MHz, $P_{out} = 110W$                   |    |     | 0.5 | dB |
| $P_{1dB}$ | Output Power at 1dB Gain Compression | Pulse width = 32 $\mu s$ , LTDC=2%, F=1030/1090 MHz |    | 110 |     | W  |
| $\eta_D$  | Drain Efficiency                     | F = 1030 MHz, $P_{out} = 110W$                      | 45 | 50  |     | %  |
| $\psi$    | Load Mismatch                        | F = 1090 MHz, $P_{out} = 110W$                      |    |     | 5:1 |    |

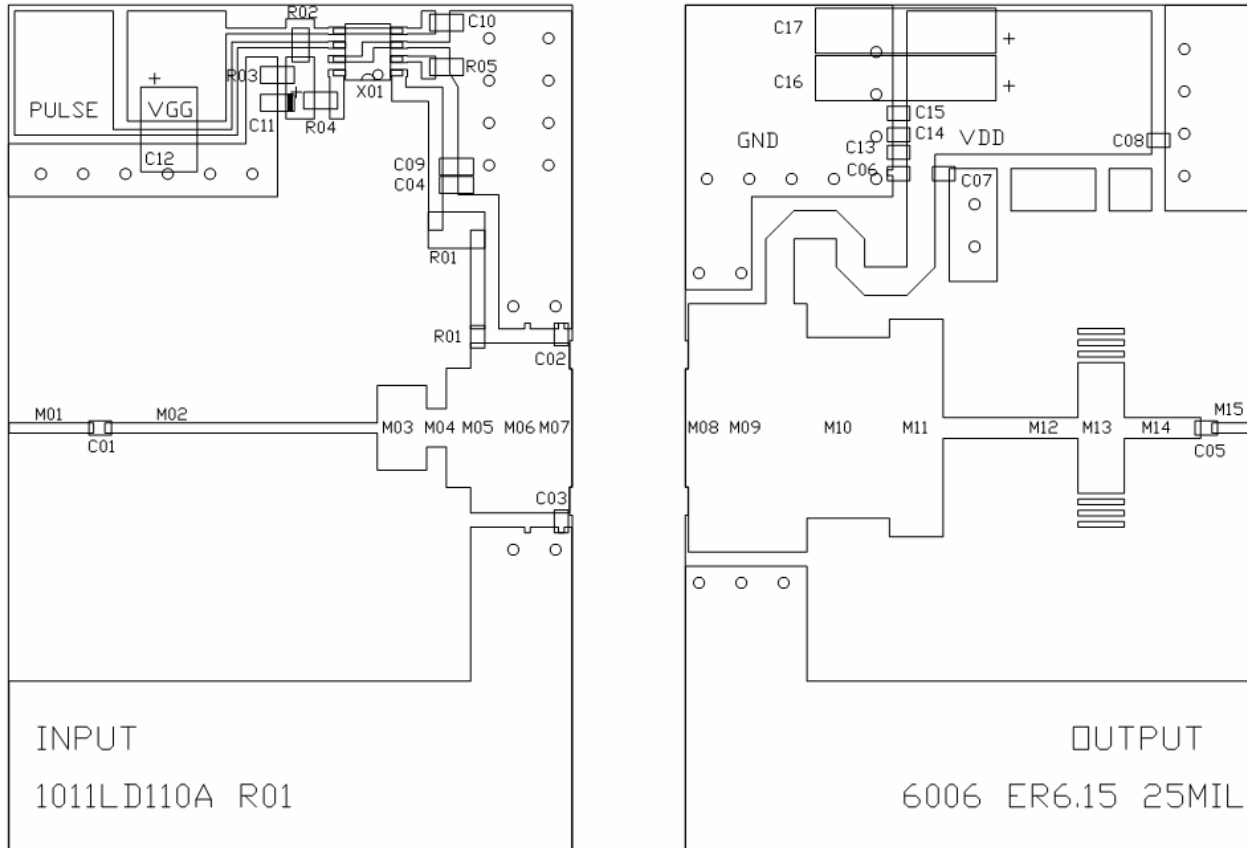
NOTES: 1. At rated output power and pulse conditions  
 2. Pulse Format 1: 32 $\mu s$ , 2% Long Term Duty Factor  
 3. Pulsed Bias:  $I_{DQ-PULSED} = 6.5mA$  (@ 42 $\mu s$  ON, 1.6msec)

Rev. 0 – Apr. 2007

## Typical Performance (1030MHz ~ 1090MHz)

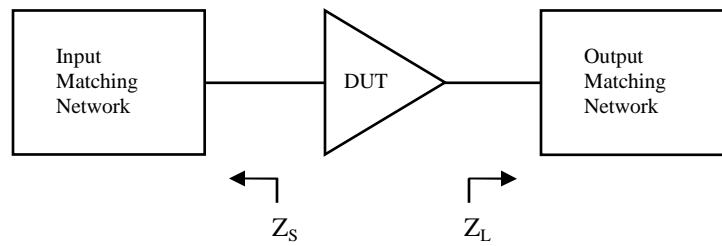


## 1011LD110A Test Circuit Layout



### 1011LD110A Test Circuit Component Designations and Values

| Part               | Description                        | Part          | Description                                      |
|--------------------|------------------------------------|---------------|--|
| C01, C04, C05, C06 | 43pF Chip Capacitor (ATC 100A)     | C10, C14, C15 | 0.033uF Chip Capacitor                           |
| C07, C08           | 100pF Chip Capacitor (ATC 100A)    | C11           | 1uF 16V Tantalum Capacitor                       |
| C02, C03           | 5.6pF Chip Capacitor (ATC 100A)    | C12           | 47uF 63V Electrolytic Capacitor                  |
| C17                | 1000uF, 63V Electrolytic Capacitor | C16           | 470uF, 63V Electrolytic Capacitor                |
| C09, C13           | 1000pF Chip Capacitor              | L01           | 6 Turns, 24 AWG, IDIA 0.092"                     |
| R01, R04           | 15Ω, 1/4W Chip Resistor            | R02, R03      | 200Ω, 1/4W Chip Resistor                         |
| R05                | 82.5Ω, 1/4W Chip Resistor          | X01           | ADG419, Analog Device                            |
| M01                | 36 x 300 mils (W x L)              | M02           | 36 x 966 mils (W x L)                            |
| M03                | 300 x 175 mils (W x L)             | M04           | 136 x 70 mils (W x L)                            |
| M05                | 422 x 86 mils (W x L)              | M06           | 602 x 351 mils (W x L)                           |
| M07                | 420 x 8 mils (W x L)               | M08           | 420 x 10 mils (W x L)                            |
| M09                | 881 x 420 mils (W x L)             | M10           | 641 x 292 mils (W x L)                           |
| M11                | 771 x 190 mils (W x L)             | M12           | 75 x 479 mils (W x L)                            |
| M13                | 464 x 164 mils (W x L)             | M14           | 75 x 271 mils (W x L)                            |
| M15                | 36 x 130 mils (W x L)              | PCB           | Rogers RT6006, ε <sub>r</sub> =6.15, 25mils, 1oz |

**Typical Impedance Values**


| Frequency (MHz) | $Z_S$ ( $\Omega$ )  | $Z_L$ ( $\Omega$ )  |
|-----------------|---------------------|---------------------|
| <b>1030</b>     | <b>0.73 - j2.71</b> | <b>3.11 - j1.66</b> |
| <b>1060</b>     | <b>0.70 - j2.49</b> | <b>2.87 - j1.79</b> |
| <b>1090</b>     | <b>0.67 - j2.28</b> | <b>2.56 - j1.82</b> |

\*  $V_{DS} = 32V$ ,  $I_{DQ} = 250mA$ ,  $P_{out} = 110W$   
 \* Pulse Format: 32 $\mu s$ , 2% Long Term Duty Factor

**Timing Diagram for Pulsed Bias**
